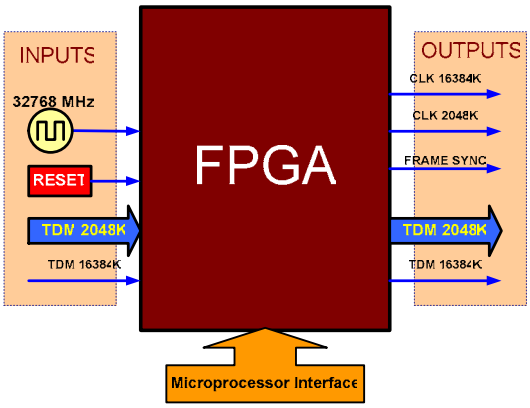
MULTI-SPEED

TIME SLOT INTERCHANGE

DIGITAL SWITCH

FEATURES:

- 512 x 512 channel non-blocking switching at 2.048 Mb/s and 16.384 Mb/s
- Input clock 32.768 MHz
- Frame Sync 125us
- Accept 8 serial data stream of 2.048 Mb/s and one serial data stream of 16.384 Mb/s
- Per-stream frame delay offset programming
- Connection memory block programming
- Microprocessor Interface



OPTIONS:

- Input clock 32.768 MHz
- Frame Sync 125us
- 0 to 3 bit frame delay
- All data received at negative edge of CLK_OUT and transmitted at positive edge of CLK_OUT
- Fit in XC2S50E XILINX FPGA

DESCRIPTIONS:

The Multi-Speed TDM Switch core is a non-blocking digital switch that has a capacity of 256 x 256 channels at 2.048 Mb/s and 256 x 256 channels at 16.384 Mb/s.

Some of the main features are: Processor Mode and input offset delay.

This IP core is synthesized for XILINX SPARTAN-IIE series FPGA, fit in XC2S50E-6TQ144 device and the post place & route simulation model simulate with Cadense NC-SIM simulator.

The Figure 1 describe the block diagram of ***MULTI-SPEED TIME SLOT ITERCHANGE DIGITAL SWITCH IP CORE***.

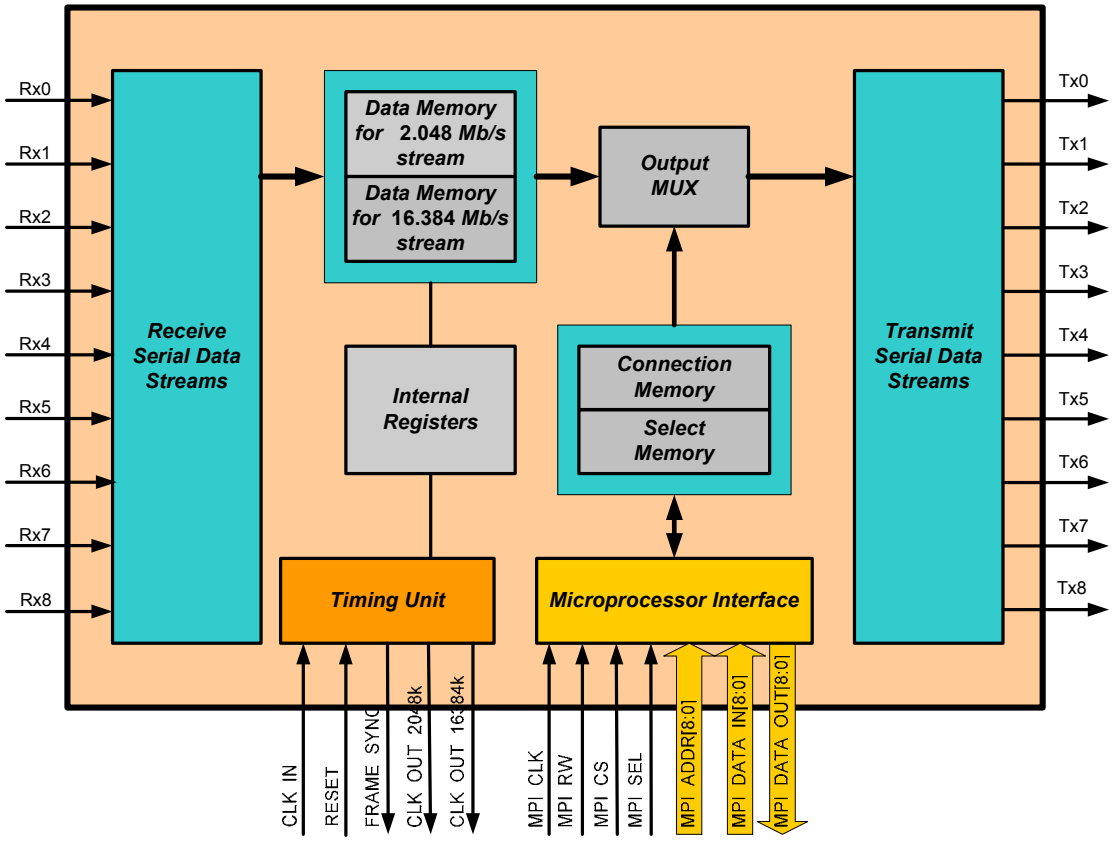


Figure 1. Block Diagram

PIN DESCRIPTION

The Table 1 is define the IP core pinout.

Table 1

SYMBOL	NAME	I/O	DESCRIPTION
CLK_IN	*Input Clock*	I	Serial clock for generation internal sync pulses. This input accept a 32.768 MHz clock
RESET	*Devise Reset*	I	This input (active LOW) put the devise in its reset state that clears the devise internal counters, registers. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the RESET pin must be held LOW for a minimum of 100ns to reset the devise.
FRAME SYNC	*Frame Sync. Signal*	O	Frame sync output. This output generates 8 KHz (125us) frame pulses.
CLOCK_OUT_2048k	*Output Clock*	O	Serial clock for shifting data in/out on the serial streams (Rx_stream_2048k/Tx_stream_2048k).This output generate 2.048 MHz clock.
CLOCK_OUT_16384k	*Output Clock*	O	Serial clock for shifting data in/out on the serial stream (Rx_stream_16384k/Tx_stream_16384k). This output generate 16.384 MHz clock.
Rx0 to Rx7	*Rx_stream_2048k*	I	Serial data input stream. These streams have a data rate of 2.048 Mb/s.
Rx8	*Rx_stream_16384k*	I	Serial data input stream. This stream have a data rate of 16.384 Mb/s.
Tx0 to Tx7	*Tx_stream_2048k*	O	Serial data output stream. These streams have a data rate of 2.048 Mb/s.
Tx8	*Tx_stream_16384k*	O	Serial data output stream. This stream have a data rate of 16.384 Mb/s.
MPI_CLK	*Memory Clock*	I	Microprocessor interface input clock. To internal connection memory and control registers accessed with positive edge of MPI_CLK.
MPI_CS	*Enable*	I	Microprocessor interface Chip Select input. The logic <0>, define access to this chip.
MPI_SEL	*Select*	I	Microprocessor interface Select input. The logic <0>, define access to control registers and logic <1>, define access to connection and select memory block.
MPI_RW	*Read / Write*	I	Microprocessor interface Read/Write input. The logic <1> is Read, <0> is Write.
MPI_ADDR	*Address [8:0]*	I	These lines provide the A8–A0 address lines to the internal memories.
MPI_DATA_IN	*Data Input [8:0]*	I	These lines provide the D8–D0 data input lines to the internal memories.
MPI_DATA_OUT	*Data Output [8:0]*	O	These lines provide the D8–D0 data output lines to the internal memories.