## Features:

- Support Spartan-II/Spartan-IIE FPGA
- 800x600 display resolution
- 16 bit color per pixel
- 72.19 Hz Frame frequency
- Up to 32 MB Video memory
- Support for 27 video pages
- Single or multi clock support
- Optimized SDRAM controller
- Host CPU to video memory access

## Applications:

- Video Games
- Security Systems

## *General Description*

The Compact Video Controller is a graphic video controller. Its functions include refreshing the display image by reading the video memory, converting the read data into a data stream acceptable for display interface, generating the control signals for display and providing the host (CPU) access to video memory.

This core with external video DAC for using with SVGA compatible CRT displays.

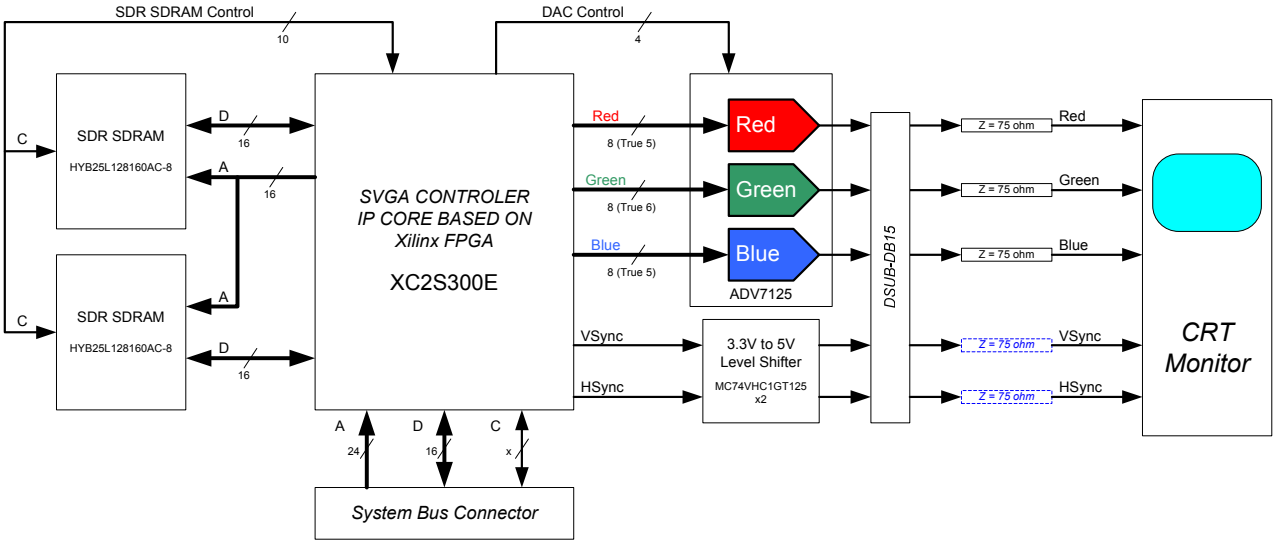


**Figure 1.**


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# *Functional Description*

The CVC core contains several functional blocks:

- Video memory controller (optimized SDRAM controller)
- Read and Write FIFO
- Video DAC Interface
- Microprocessor Interface
- Video Sync Generator
- Control Unit
- Clock DLL

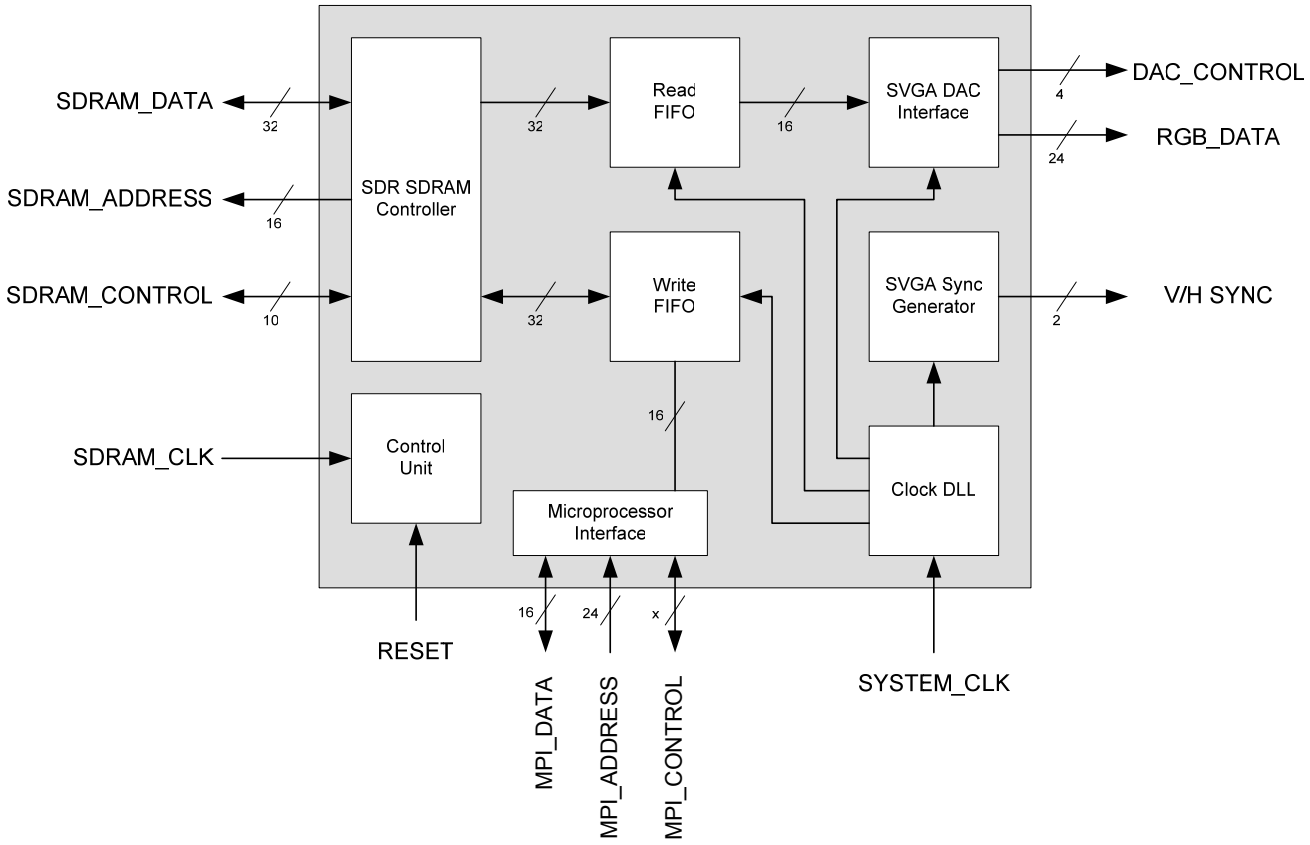


**Figure 2.**


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## *Timing Diagram*

The Figure 3 show output video sync pulses and its timing parameters for 800x600 16bit SVGA display supported by CVC core.

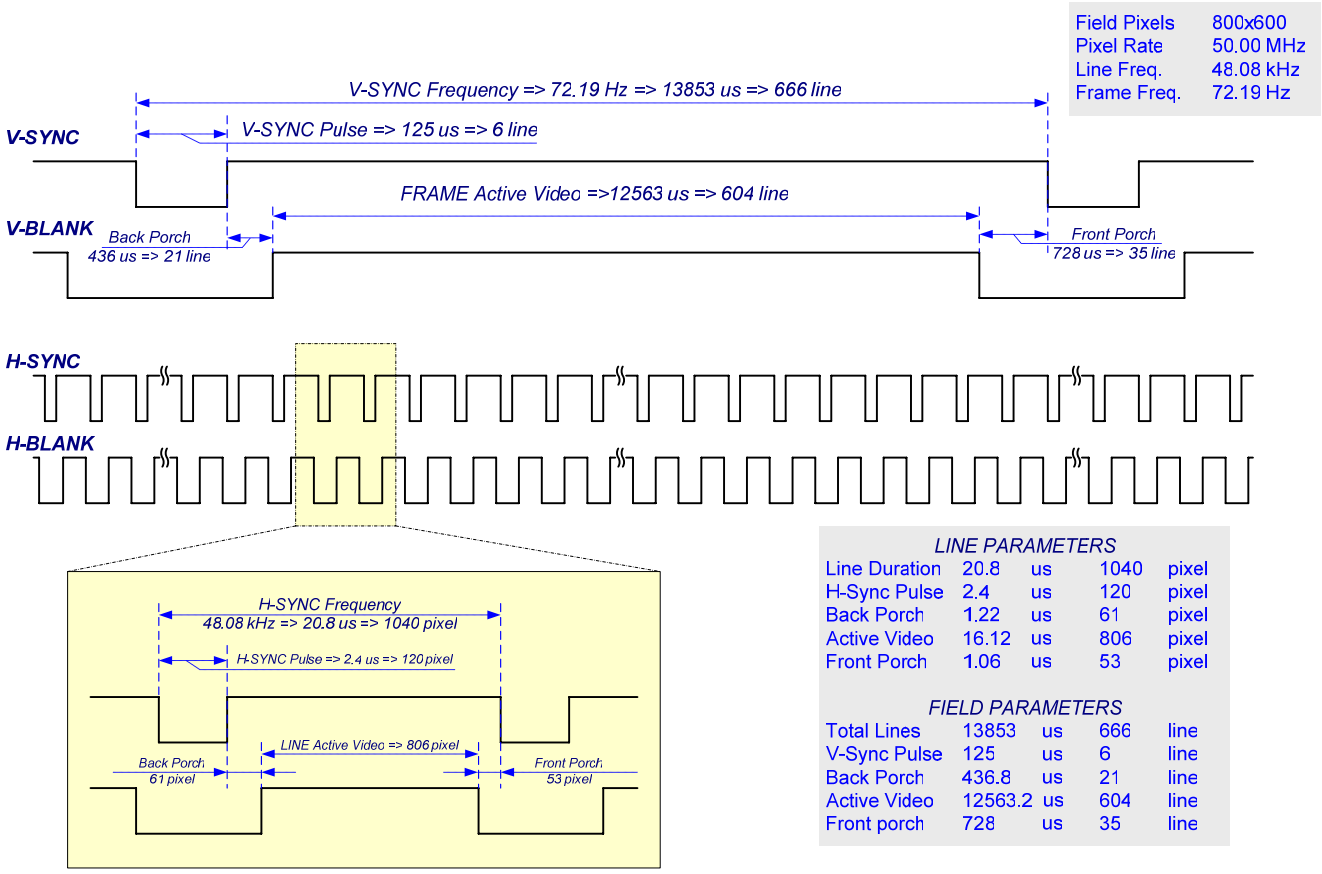


**Figure 3.**


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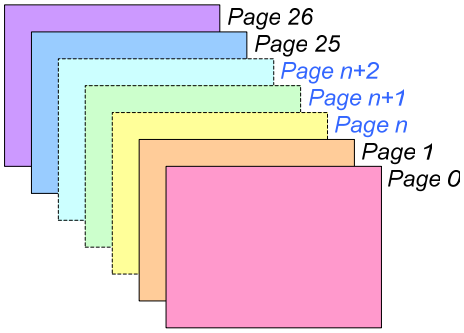
## *Video Memory Organization*

The video memory controller can support up to 32 MB SDRAM. This memory contains 27 visible video frames. The structure of memory addressing is shown in Figure 4.

| | Phisical Address | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit # | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit # | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| | Page Number + Line Address in Page | | | | | | | | | | | | | | Pixel Address in Line | | | | | | | | |




**VIDEO MEMORY MAP**

| Page # | Start Addr | End Addr |
|---|---|---|
| 0 | {14'd0, 9'd0} | {14'd603, 9'd511} |
| 1 | {14'd604, 9'd0} | {14'd1207, 9'd511} |
| 2 | {14'd1208, 9'd0} | {14'd1811, 9'd511} |
| 3 | {14'd1812, 9'd0} | {14'd2415, 9'd511} |
| 25 | {(Page# * 10'd604), 9'd0} | {(((Page#+1) * 10'd604)-1), 9'd511} |
| 26 | {(Page# * 10'd604), 9'd0} | {(((Page#+1) * 10'd604)-1), 9'd511} |

***page_line_addr[14:0] = page_number[4:0] * line_number[9:0]***
***(800x600 Mode >>> page_number = 0-:-26, line_number = 604)***

***video_ram_addr[22:0] = {page_line_addr[13:0], line_pixel_addr[8:0]}***

**Figure 4.**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