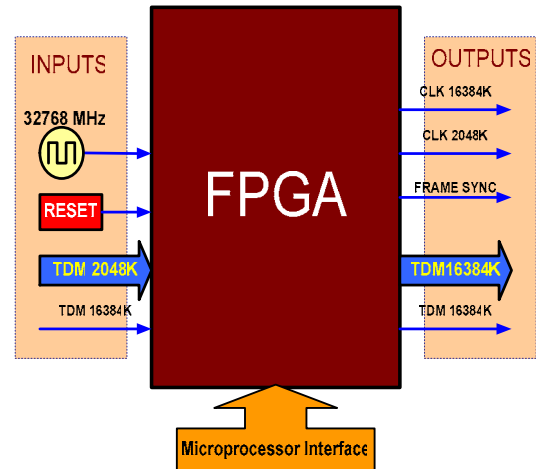


MULTI-SPEED
TIME SLOT INTERCHANGE
DIGITAL SWITCH
512 x 512

FEATURES:

- 512 x 512 channel non-blocking switching at 2.048 Mb/s and 16.384 Mb/s
- Input clock 32.768 MHz
- Frame Sync 125us
- Accept 8 serial data stream of 2.048 Mb/s and one serial data stream of 16.384 Mb/s
- Per-stream frame delay offset programming
- Connection memory block programming
- Microprocessor Interface

**OPTIONS:**

- Input clock 32.768 MHz
- Frame Sync 125us
- 0 to 3 bit frame delay
- All data received at negative edge of CLK_OUT and transmitted at positive edge of CLK_OUT
- Fit in XC2S50E XILINX FPGA

DESCRIPTIONS:

The Multi-Speed TDM Switch core is a non-blocking digital switch that has a capacity of 256 x 256 channels at 2.048 Mb/s and 256 x 256 channels at 16.384 Mb/s.

Some of the main features are: Processor Mode and input offset delay.

This IP core is synthesized for XILINX SPARTAN-IIE series FPGA, fit in XC2S50E-6TQ144 device and the post place & route simulation model simulate with Cadence NC-SIM simulator.

The **Figure 1** describe the block diagram of **MULTI-SPEED TIME SLOT ITERCHANGE DIGITAL SWITCH IP CORE**.

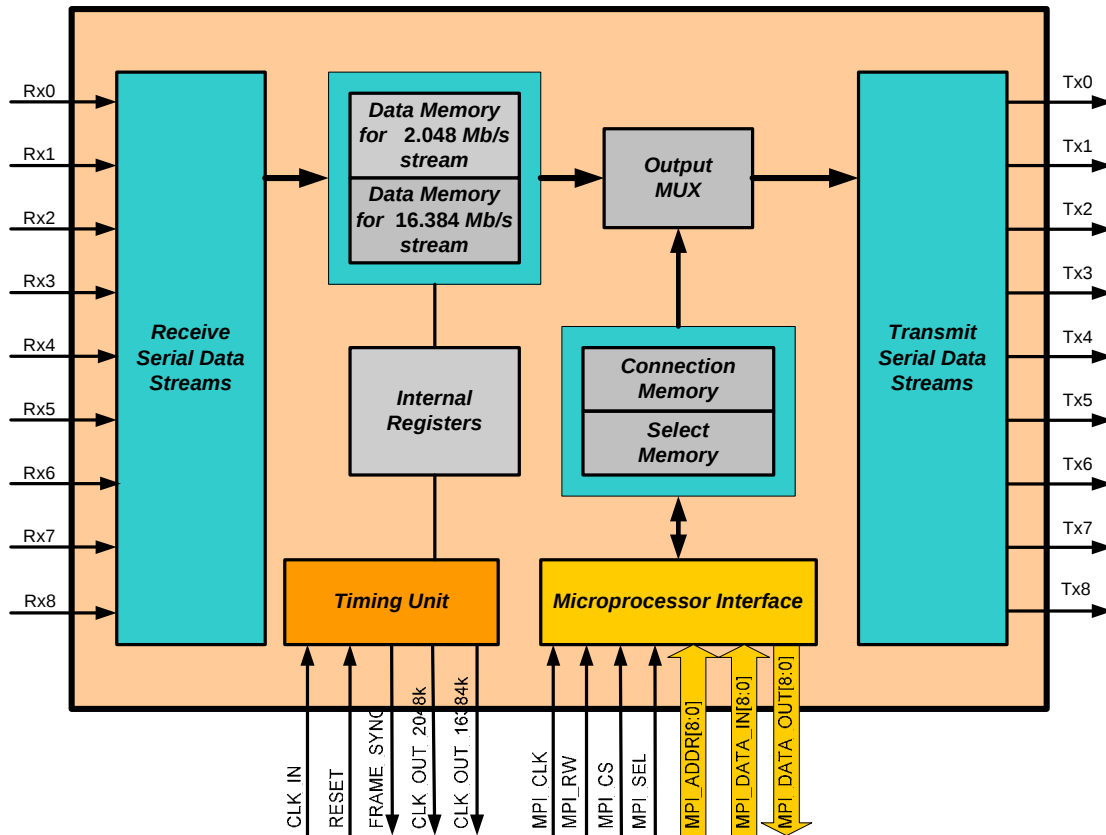


Figure 1. Block Diagram

PIN DESCRIPTION

The **Table 1** is defining the IP core pinout.

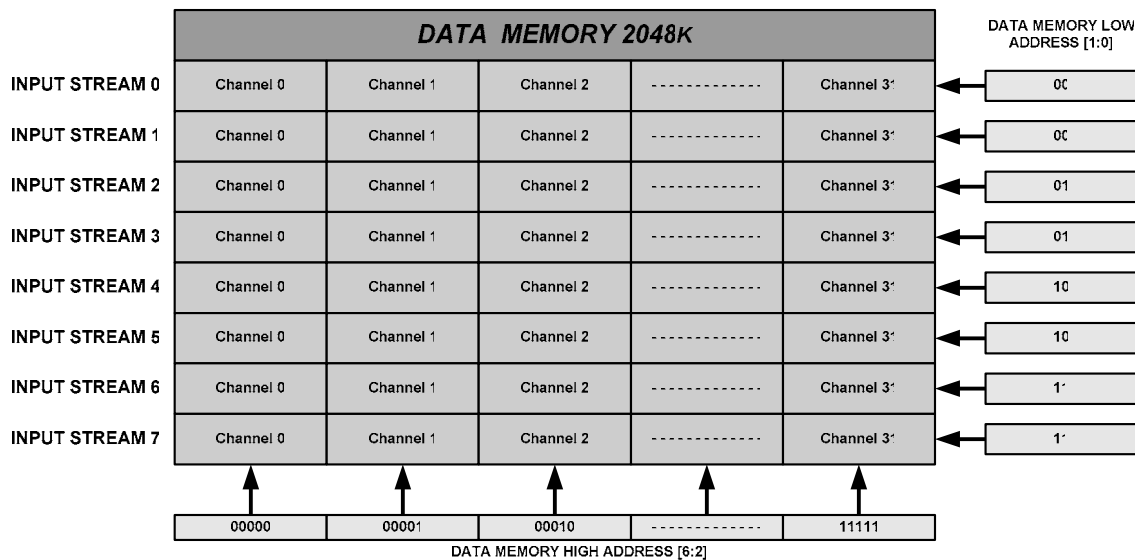
Table 1

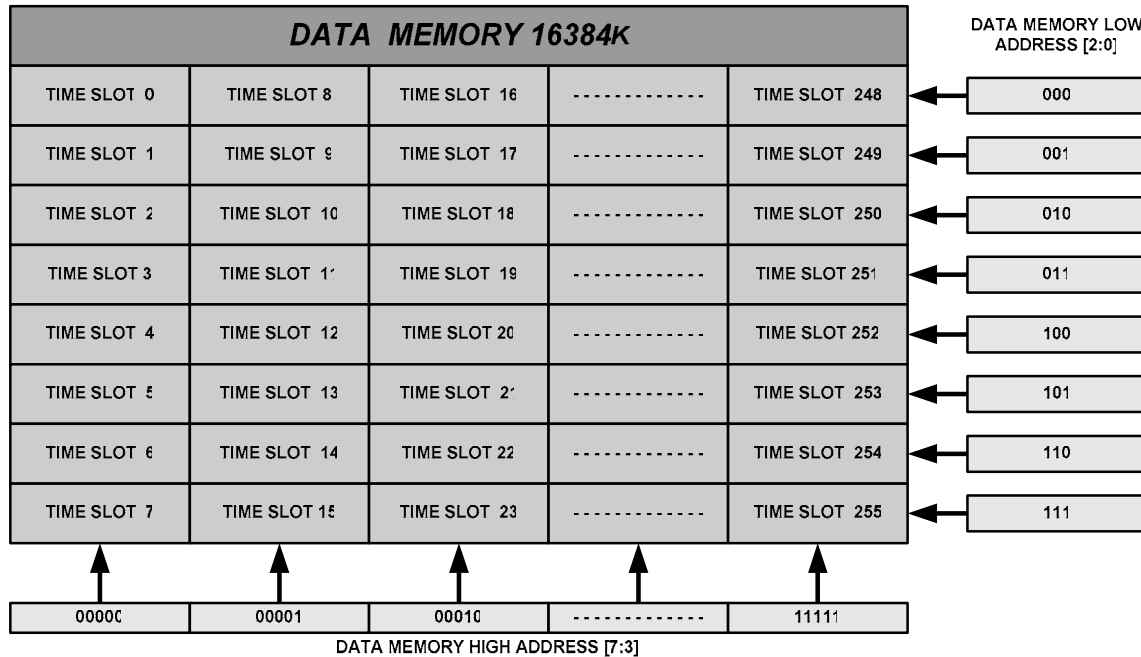
SYMBOL	NAME	I/O	DESCRIPTION
CLK_IN	<i>Input Clock</i>	I	Serial clock for generation internal sync pulses. This input accept a 32.768 MHz clock
RESET	<i>Devise Reset</i>	I	This input (active LOW) put the devise in its reset state that clears the devise internal counters, registers. The time constant for a power up reset circuit must be a minimum of five times the rise time of the power supply. In normal operation, the RESET pin must be held LOW for a minimum of 100ns to reset the devise.
CLOCK_OUT_2048k	<i>Output Clock</i>	O	Serial clock for shifting data in/out on the serial streams (Rx_stream_2048k/Tx_stream_2048k).This output generate 2.048 MHz clock.
CLOCK_OUT_16384k	<i>Output Clock</i>	O	Serial clock for shifting data in/out on the serial stream (Rx_stream_16384k/Tx_stream_16384k). This output generate 16.384 MHz clock.
Rx_stream_2048k	<i>Rx Input 0 to 7</i>	I	Serial data input stream. These streams have a data rate of 2.048 Mb/s.
Rx_stream_16384k	<i>Rx Input</i>	I	Serial data input stream. This stream have a data rate of 16.384 Mb/s.
FRAME_SYNC	<i>Frame Sync. Signal</i>	O	Frame sync output. This output generate 8 KHz (125us) frame pulses.
Tx_stream_2048k	<i>Tx Output 0 to7</i>	O	Serial data output stream. These streams have a data rate of 2.048 Mb/s.
Tx_stream_16384k	<i>Tx Output</i>	O	Serial data output stream. This stream have a data rate of 16.384 Mb/s.
MPI_CLK	<i>Memory Clock</i>	I	Microprocessor interface input clock. To internal connection memory and control registers accessed with positive edge of MPI_CLK.
MPI_CS	<i>Enable</i>	I	Microprocessor interface Chip Select input. The logic <0>, define access to this chip.
MPI_SEL	<i>Select</i>	I	Microprocessor interface Select input. The logic <0>, define access to control registers and logic <1>, define access to connection and select memory block.
MPI_RW	<i>Read / Write</i>	I	Microprocessor interface Read/Write input. The logic <1> is Read, <0> is Write.
MPI_ADDR	<i>Address [8:0]</i>	I	These lines provide the A8–A0 address lines to the internal memories.
MPI_DATA_IN	<i>Data Input [8:0]</i>	I	These lines provide the D8–D0 data input lines to the internal memories.
MPI_DATA_OUT	<i>Data Output [8:0]</i>	O	These lines provide the D8–D0 data output lines to the internal memories.

MEMORY MAP

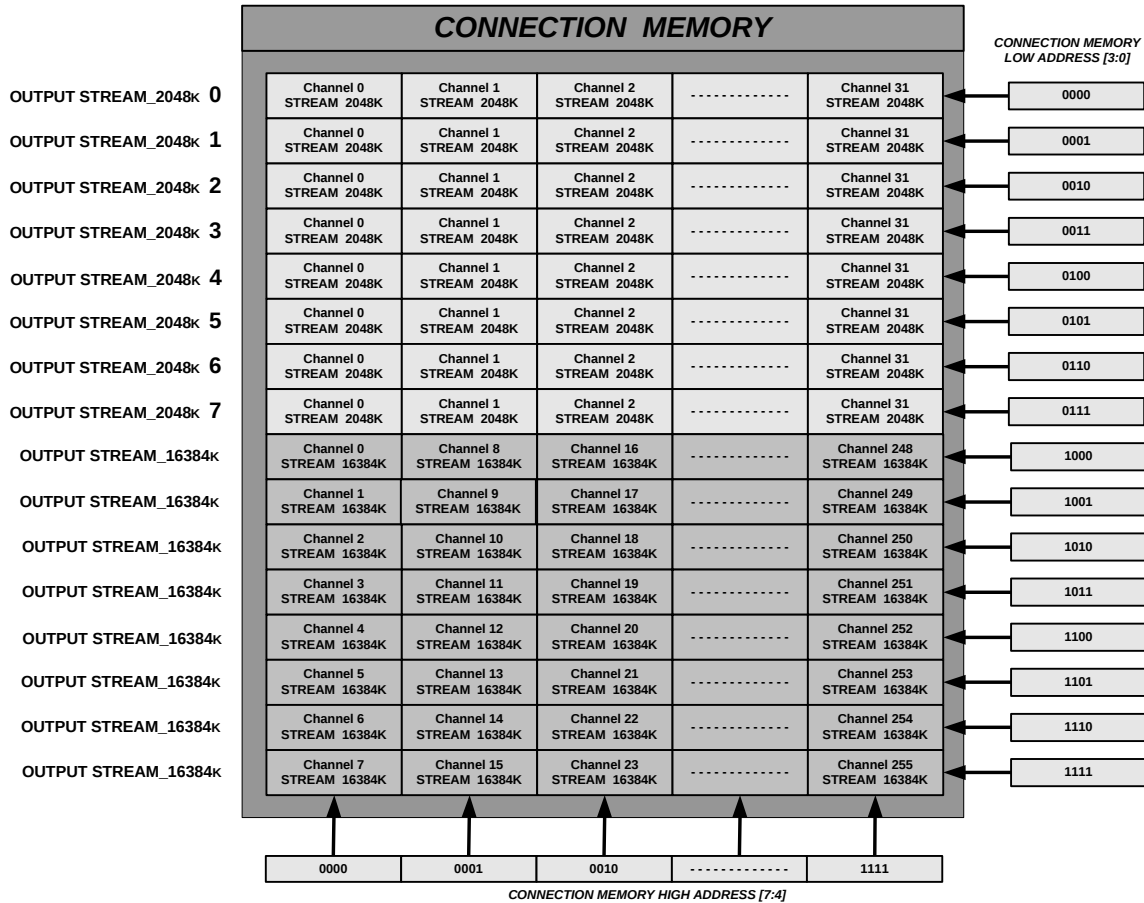
The IP core consist of two memory DATA and CONNECTION.

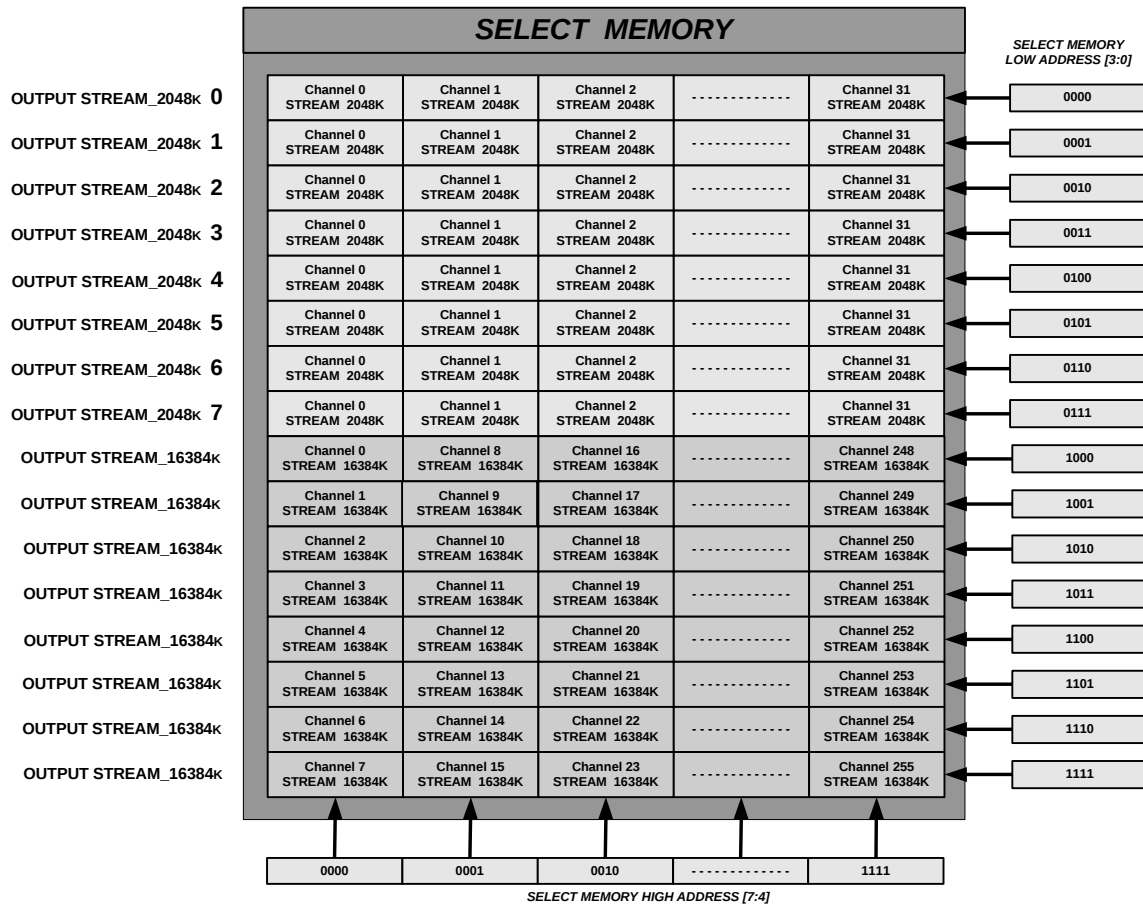
The DATA memory consist four banks of memories. In first frame the data from input streams with data rate 2.048 Mb/s stored in the data memory **Bank 1**, and the data from input stream with data rate 16.384 Mb/s stored in the data memory **Bank 3**. At this time the data from data memory **Bank 2** and **Bank 4** select depending are transmitted to output streams. In second frame the data memory banks are swap around.



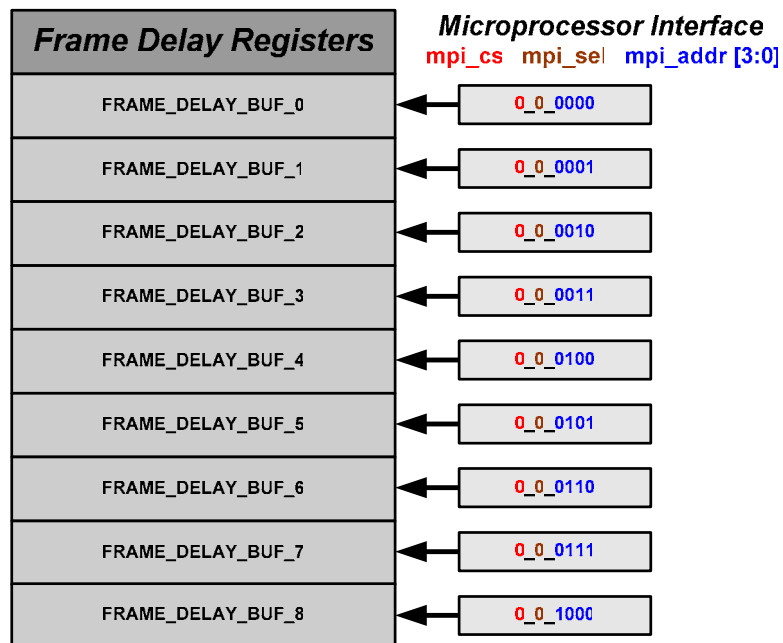


The CONNECTION memory consists is a two part SELECT and CONNECTION and loaded from microprocessor interface (MPI) and consist information about connection between data memory and output streams.





The FRAME DELAY REGISTERS also loaded from MPI. This registers are responsible to frame delay for each input stream correspondingly.



The Multi-Speed Time Slot Interchange Digital Switch IP core files

NAME	DESCRIPTION
MS-TDM_Switch_DS.pdf	Data Sheet file
ms_tdm_switch_top.v	Top module of Multi-Speed Time Slot Interchange Digital Switch
ms_tdm_switch_b.v	Top module of Multi-Speed Time Slot Interchange Digital Switch for behavioral simulation
test_ms_tdm_switch_top.v	Testbench for top module
map.dat	Data file for connection memory (line 1 - 512) and frame delay registers (line 513 - 521)
stream_0.dat	Data for input stream 0 (2.048 MHz)
stream_1.dat	Data for input stream 1 (2.048 MHz)
stream_2.dat	Data for input stream 2 (2.048 MHz)
stream_3.dat	Data for input stream 3 (2.048 MHz)
stream_4.dat	Data for input stream 4 (2.048 MHz)
stream_5.dat	Data for input stream 5 (2.048 MHz)
stream_6.dat	Data for input stream 6 (2.048 MHz)
stream_7.dat	Data for input stream 7 (2.048 MHz)
stream_8.dat	Data for input stream 8 (16.384 MHz)
sim_result_2048k.dat	Simulation result file for 2.048 Mb/s data rate streams created by testbench “test_ms_tdm_switch_top.v ”
sim_result_16384k.dat	Simulation result file for 16.384 Mb/s data rate stream created by testbench “test_ms_tdm_switch_top.v ”

